CLAIMS

What is claimed is:

1. A circuit comprising:

an integration capacitor coupled to an integration node;

a comparator having a first input coupled to the integration node and a second input coupled to a first reference voltage V_{ref1};

a dump capacitor having a first node and a second node;

a transistor having a first node coupled through a first switch to said integration node, said transistor having an opposed second node coupled to said first node of the dump capacitor and a third node coupled to a second reference voltage V_{ref2}; and

a second switch disposed across the dump capacitor;

where open and closed states of said first and second switches are controlled by an output of the comparator.

2. The circuit of claim 1 wherein said comparator operates to maintain the first switch open and the second switch closed when in a first comparator state, and further operates to maintain the first switch closed and the second switch open when in a second comparator state.

3. The circuit of claim 1 wherein the transistor comprises a field effect transistor FET.

4. The circuit of claim 3 wherein the FET first node comprises a drain, the FET second node comprises a source, and the third node comprises a gate.

5. The circuit of claim 1 wherein said integration node and said integration capacitor are coupled to a radiation detector.

6. The circuit of claim 5 wherein said radiation detector operates as a current source to said circuit.

7. The circuit of claim 1 wherein a voltage V_{int} at the integration node is never less than the second reference voltage V_{ref2}.

8. The circuit of claim 1 wherein the comparator is restricted to changing states only on a clock edge.

9. The circuit of claim 8 further comprising a counter coupled to an output of the comparator.

10. The circuit of claim 1 further comprising a residue readout coupled to the integration node.

11. A readout circuit comprising:

an input node for receiving a signal from a radiation detector;

an integrating capacitor having a first node coupled to the input node;

a comparator having a first input coupled to said integrating capacitor first node and a second input coupled to a first reference signal;

an injection field effect transistor FET having a gate coupled to a second reference signal, said FET coupled between said integrating capacitor first node and a node of a dump capacitor;

a first switch disposed between the injection FET and the integrating capacitor first node; and

a second switch across said dump capacitor;

wherein an output of said comparator is coupled to said first and second switches for operating said switches in opposition to one another.

12. The readout circuit of claim 11 in combination with a radiation sensor having an output coupled to the input node.

13. A plurality of *n* readout circuits of claim 11 disposed on a first substrate in combination with a plurality of radiation sensors disposed on a second substrate, said first and second substrate in fixed relation to one another and coupled such that the input node of each of the *n* readout circuits is coupled to an output of a radiation sensor.

14. A method for converting an analog signal to a digital signal comprising:

inputting an analog current signal to an input node;

comparing an electrical parameter at an integration node to a reference electrical parameter;

when in a first comparator state, charging a capacitor from the input node such that a charge on the capacitor represents an integral of the analog current signal at the input node;

when in a second comparator state, decrementing the charge on the capacitor; and

counting a number of decrements.

15. The method of claim 14 wherein decrementing the capacitor comprises transferring a fixed amount of charge from said capacitor.

16. The method of claim 15 wherein the fixed amount of charge is transferred from the said capacitor to a dump capacitor via an injection FET.

17. The method of claim 16 wherein a gate voltage V_{ref2} of the injection FET is less than a minimum voltage $V_{int}(min)$ at the integration node.

18. The method of claim 14 wherein comparing an electrical parameter comprises actuating two switches in opposition to effect the method for the first and second comparator states.